WHAT IS CLAIMED IS:

1. A process of manufacturing a semiconductor device, comprising:

plasma etching through a patterned hardmask layer located over a semiconductor substrate wherein said plasma etching forms a modified layer on said hardmask layer; and

removing at least a substantial portion of said modified layer by exposing said modified layer to a post plasma clean process.

2. The process as recited in Claim 1 wherein said removing includes exposing said modified layer to an isotropic etch.

3. The process as recited in Claim 2 wherein said isotropic etch includes phosphoric acid.

4. The process as recited in Claim 1 wherein plasma etching includes etching through a patterned silicon, silicon nitride, silicon carbide or oxynitride hardmask.

5. The process as recited in Claim 1 further including removing a photoresist layer from said patterned hardmask prior to said plasma etching.

6. The process as recited in Claim 1 wherein removing includes removing all of said modified layer to thereby leave an unmodified hardmask layer.

7. The process as recited in Claim 1 wherein said plasma etching further includes forming a trench in said semiconductor substrate prior to said removing.

8. The process as recited in Claim 7 further including forming an oxide liner in said trench.

9. The process as recited in Claim 8 wherein forming said oxide liner includes forming said oxide liner prior to said removing.

10. The process as recited in Claim 1 wherein removing includes removing an upper thickness of said patterned hardmask layer ranging from about 3 nm to about 24 nm.

11. A process of manufacturing an integrated circuit, comprising:

forming isolation trenches in a semiconductor substrate, including:

plasma etching through a patterned hardmask layer located over a semiconductor substrate wherein said plasma etching forms a modified layer on said hardmask layer; and

removing at least a substantial portion of said modified layer by exposing said modified layer to a post plasma clean process;

forming transistor structures on and within said substrate and between said isolation trenches; and

forming interconnects within dielectric layers located over said transistors structures that interconnect said transistor structures to form an operative integrated circuit.

12. The process as recited in Claim 11 wherein said removing includes exposing said modified layer to an isotropic etch.

13. The process as recited in Claim 12 wherein said isotropic etch includes phosphoric acid.

14. The process as recited in Claim 11 wherein plasma etching includes etching through a patterned hardmask comprising silicon or

nitrogen.

15. The process as recited in Claim 11 further including removing a photoresist layer from said patterned hardmask prior to said plasma etching.

16. The process as recited in Claim 11 wherein removing includes removing all of said modified layer to thereby leave an unmodified hardmask layer.

17. The process as recited in Claim 11 further including forming an oxide liner in said trench.

18. The process as recited in Claim 17 wherein forming said oxide liner includes forming said oxide liner prior to said removing.

19. The process as recited in Claim 11 wherein exposing includes removing an upper thickness of said patterned hardmask layer ranging from about 3 nm to about 24 nm.

20. The process as recited in Claim 11 wherein forming transistor structures includes forming a gate on said semiconductor substrate and forming wells and source/drain regions within said

substrate.